

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: **Mitsuaki HORI, et al.**

Serial Number: **Not Yet Assigned**

Filed: **September 16, 2003**

For: **SEMICONDUCTOR DEVICE, MANUFACTURE AND EVALUATION METHODS  
FOR SEMICONDUCTOR DEVICE, AND PROCESS CONDITION EVALUATION  
METHOD**

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

September 16, 2003

Sir:

In compliance with 37 CFR 1.56, Applicants call to the attention of the Patent and Trademark

Office the reference listed on the attached PTO-1449.

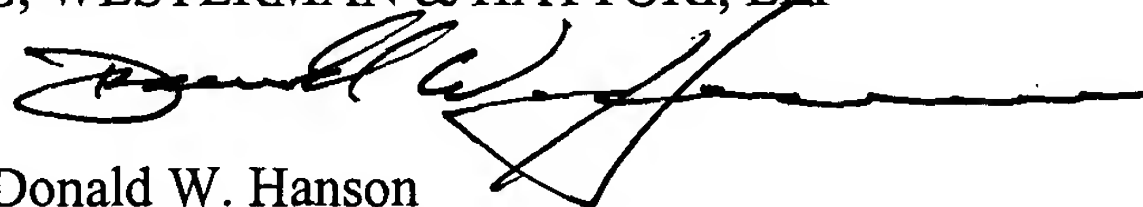
A copy of the reference, except for the U.S. patent reference, is enclosed herewith.

In the event there are any fees due in connection with the filing of this paper, please charge

Deposit Account No. 01-2340.

Respectfully submitted,

**ARMSTRONG, WESTERMAN & HATTORI, LLP**



Donald W. Hanson  
Attorney for Applicants  
Reg. No. 27,133

DWH/jaz  
Atty. Docket No. **031111**  
Suite 1000  
1725 K Street, N.W.  
Washington, D.C. 20006  
(202) 659-2930



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**PATENT TRADEMARK OFFICE**

Enclosures: PTO-1449; References (1)

<b>INFORMATION DISCLOSURE STATEMENT PTO-1449</b>	Atty. Docket No. 031111	Serial No. <b>New Application</b>
	Applicant(s): <b>Mitsuaki HORI, et al.</b>	
	Filing Date: <b>September 16, 2003</b>	Group Art Unit: <b>Not Yet Assigned</b>

### U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA	6,215,146	Umeda et al.	04/10/01			
_____	AB						
_____	AC						
_____	AD						

### FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Translation (Yes or No)
_____	AE	11-204787	07/30/99	Japan	Yes-Abstract/Discussed in the specification
_____	AF				
_____	AG				
_____	AH				
_____	AI				

### OTHER DOCUMENTS

_____	AJ	
_____	AK	
Examiner		Date Considered